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In re the Patent Application of: **Seong-Hoon Lee** Serial No. 10/750,602 Filed: December 29, 2003 For: **SYNCHRONOUS MEMORY DEVICE HAVING ADVANCED DATA ALIGN CIRCUIT**	Examiner: Paul W. Schlie Art Unit: 2186

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AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended): A semiconductor device comprising:

a data strobe buffering means for generating N number of align control signals based on a data strobe signal and an external clock signal, including a strobe signal divider for receiving the data strobe signal to generate N number of the align control signals based on the data strobe signal sequence;

a receiving block in response to N-1 number of the align control signals for receiving the plurality of input data and outputting intermediate N-bit data in a parallel fashion; and

an outputting block in response to the remaining align control signal for receiving the intermediate N-bit data in the parallel fashion and outputting the intermediate N-bit data in synchronization with the remaining align control signal having an N/2 external clock period to generate the synchronized intermediate N-bit data as the N-bit output data,

wherein the semiconductor device operates to receive a plurality of input data to output the N-bit output data at one clock, N being a positive integer, and N is at least 4,

wherein the data strobe buffering means generates the N number of align control signals, each having an N/2 external clock period, the receiving block includes N-1 number of latch blocks in response to the N-1 number of the align control signals, and the data strobe buffering

means includes:

an instruction decoder for generating an initialization pulse for initializing the strobe signal divider in response to the data strobe signal.

Claims 2-4 (Canceled)

Claim 5 (Currently Amended): The semiconductor device as recited in ~~claim 3~~claim 1, wherein the receiving block includes:

a first latching block for receiving 2-bit data and outputting the 2-bit data in synchronization with a first align control signal to generate the synchronized 2-bit data as a first synchronized data;

a second latching block for receiving the first synchronized data and outputting the first synchronized data in synchronization with a second align control signal to generate the synchronized as some of the intermediate N-bit data; and

a third latching block for receiving 2-bit data and outputting the 2-bit data in synchronization with a third align control signal to generate the synchronized 2-bit data as the other of the intermediate N-bit data.

Claim 6 (Previously Presented): The semiconductor device as recited in claim 5, wherein each of the first to third latching blocks includes at least one latch for synchronizing 1-bit data with one of the align control signals.

Claim 7 (Canceled):

Claim 8 (Currently Amended): The semiconductor device as recited in ~~claim 7~~claim 1, wherein the strobe signal divider includes:

first to forth strobe pulse generators, each for receiving the data strobe signal and generating the align control signals based on the strobe signal sequence; and

an initial setting block for initializing the first to forth strobe pulse generators,

wherein the align control signal has the N/2 external clock period.

Claim 9 (Currently Amended): The semiconductor device as recited in ~~claim 7~~claim 1, wherein the data strobe buffering means includes a latency shifter coupled between the instruction decoder and the strobe signal divider for delaying the initialization pulse for a predetermined time.

Claim 10 (Currently Amended): The semiconductor device as recited in ~~claim 7~~claim 1, wherein the data strobe buffering means includes a strobe signal buffer for receiving the data strobe signal and outputting the data strobe signal to the strobe signal divider.

Claims 11-13 (Canceled)

Claim 14 (Previously Presented): The semiconductor device as recited in ~~claim 12~~claim 1, wherein the receiving block includes:

a first latching block for receiving 2-bit data and outputting the 2-bit data in synchronization with a first align control signal to generate the synchronized 2-bit data as a first synchronized data;

a second latching block for receiving the first synchronized data and outputting the first synchronized data in synchronization with a second align control signal to generate the synchronized data as some of the intermediate N-bit data; and

a third latching block for receiving the synchronized 2-bit data outputted from the second latching block and outputting the 2-bit data in synchronization with a third align control signal to generate the synchronized 2-bit data as the other of the intermediate N-bit data.

Claim 15 (Original): The semiconductor device as recited in claim 14, wherein each of the first to third latching blocks includes at least one latch for synchronizing 1-bit data with one of the align control signals.

Claim 16 (Cancelled)

Claim 17 (Currently Amended): The semiconductor device as recited in ~~claim 12~~claim 1, wherein the data strobe buffering means includes:

an instruction decoder for generating an initialization pulse for initializing the strobe signal divider in response to the data strobe signal.

Claim 18 (Original): The semiconductor device as recited in claim 17, wherein the strobe signal divider includes:

first to forth strobe pulse generators, each for receiving the data strobe signal and generating the align control signals based on the strobe signal sequence; and

an initial setting block for initializing the first to forth strobe pulse generators,

wherein the align control signal has the N/2 external clock period.

Claim 19 (Original): The semiconductor device as recited in claim 17, wherein the data strobe buffering means includes a latency shifter coupled between the instruction decoder and the strobe signal divider for delaying the initialization pulse for a predetermined time.

Claim 20 (Previously Presented): The semiconductor device as recited in claim 17, wherein the data strobe buffering means includes a strobe signal buffer for receiving the data strobe signal and outputting the data strobe signal to the strobe signal divider.

Claim 21 (Previously Presented): The semiconductor device as recited in claim 1, wherein the outputting block includes N number of latches, each for synchronizing the intermediate N-bit data with the remaining align control signal having the N/2 external clock period to generate the synchronized intermediate N-bit data as the N-bit output data.

Claim 22 (Previously Presented): The semiconductor device as recited in claim 1, further comprising a global input-output driver for generating the N-bit output data in response to the strobe enable signal.

Claim 23 (New): A semiconductor device comprising:

a data strobe buffering means for generating N number of align control signals based on a data strobe signal and an external clock signal, including a strobe signal divider for receiving the data strobe signal to generate N number of the align control signals based on the data strobe signal sequence;

a receiving block in response to N-1 number of the align control signals for receiving the plurality of input data and outputting intermediate N-bit data in a parallel fashion; and

an outputting block in response to the remaining align control signal for receiving the intermediate N-bit data in the parallel fashion and outputting the intermediate N-bit data in synchronization with the remaining align control signal having an N/2 external clock period to generate the synchronized intermediate N-bit data as the N-bit output data,

wherein the semiconductor device operates to receive a plurality of input data to output the N-bit output data at one clock, N being a positive integer, and N is at least 4,

wherein the data strobe buffering means generates the N number of align control signals, at least one having an N/2 external clock period, the receiving block includes N-1 number of latch blocks in response to the N-1 number of the align control signals, and the data strobe buffering means includes:

an instruction decoder for generating an initialization pulse for initializing the strobe signal divider in response to the data strobe signal.

Claim 24 (New): The semiconductor device as recited in claim 23, wherein the strobe signal divider includes:

first to forth strobe pulse generators, each for receiving the data strobe signal and generating the align control signals based on the strobe signal sequence; and

an initial setting block for initializing the first to forth strobe pulse generators,

wherein the align control signal has the N/2 external clock period.

Claim 25 (New): The semiconductor device as recited in claim 23, wherein the data strobe buffering means includes a latency shifter coupled between the instruction decoder and the strobe signal divider for delaying the initialization pulse for a predetermined time.

Claim 26 (New): The semiconductor device as recited in claim 23, wherein the data strobe buffering means includes a strobe signal buffer for receiving the data strobe signal and outputting the data strobe signal to the strobe signal divider.